FIG. 1

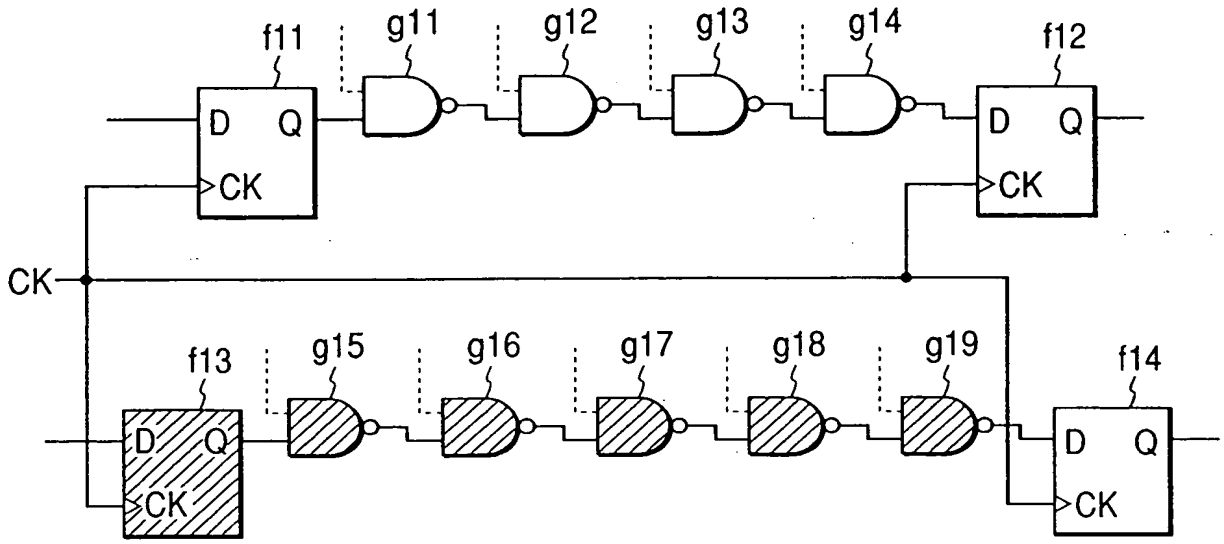
f11
g11
g12
g13
g14
f12
D
Q
CK
CK
f13
g15
g16
g17
g18
g19
f14

FIG. 2

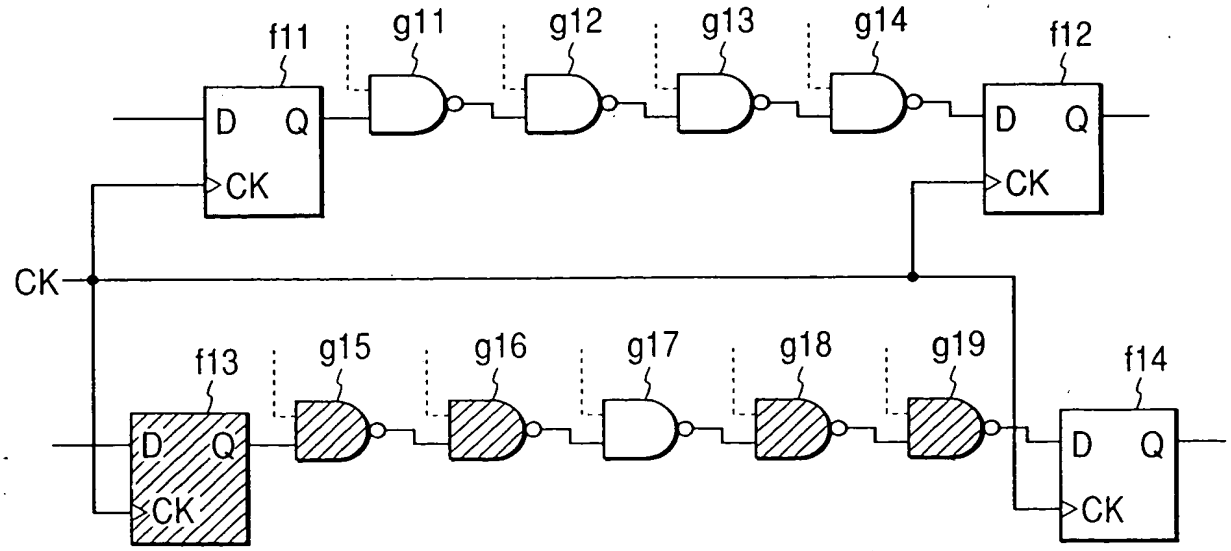
f11
g11
g12
g13
g14
f12
D
Q
CK
CK
f13
g15
g16
g17
g18
g19
f14

FIG. 3

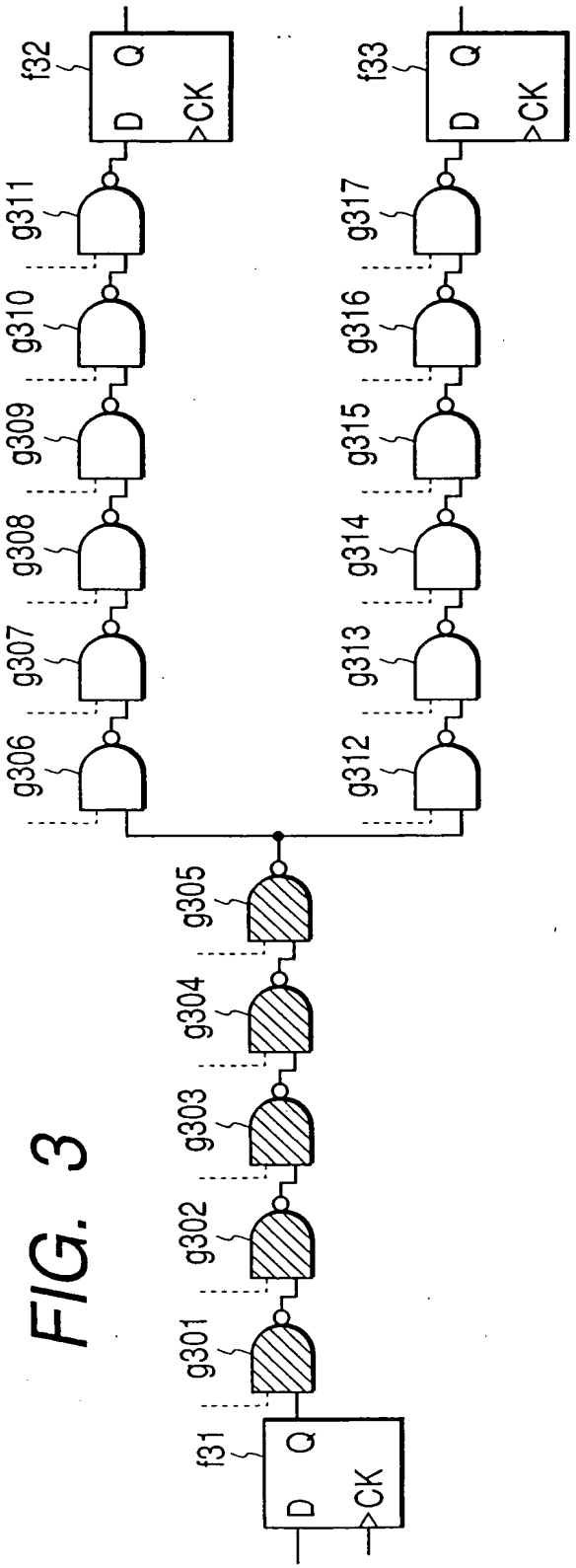
f31
f32
f33
g301
g302
g303
g304
g305
g306
g307
g308
g309
g310
g311
g312
g313
g314
g315
g316
g317
D
Q
CK

FIG. 4

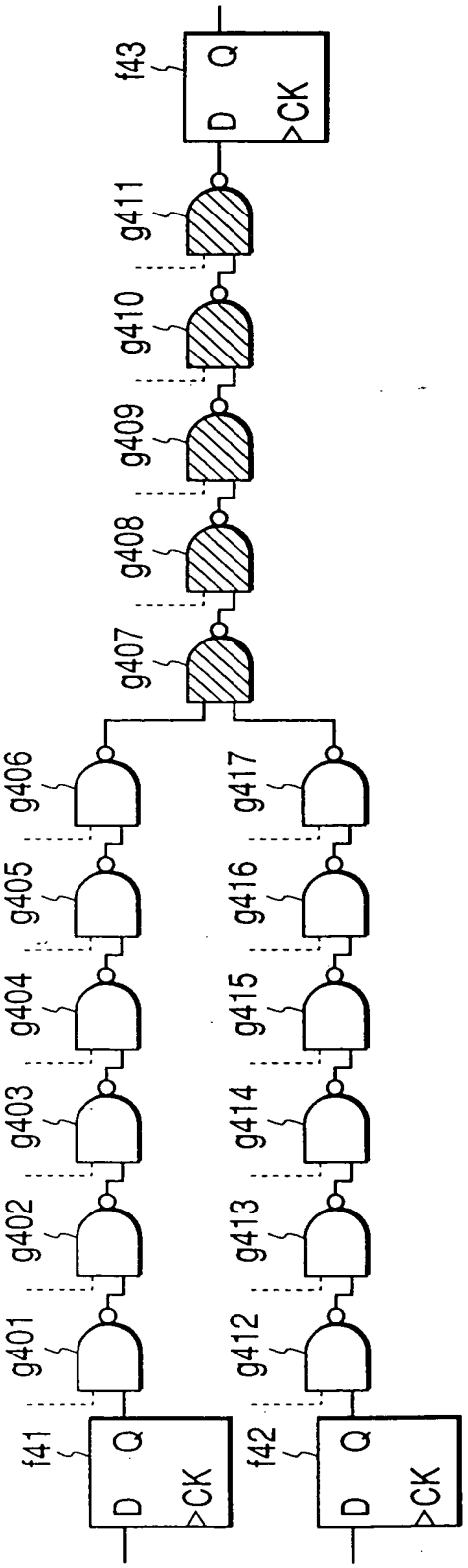
f41
f42
f43
g401
g402
g403
g404
g405
g406
g407
g408
g409
g410
g411
g412
g413
g414
g415
g416
g417
D
Q
CK

FIG. 5

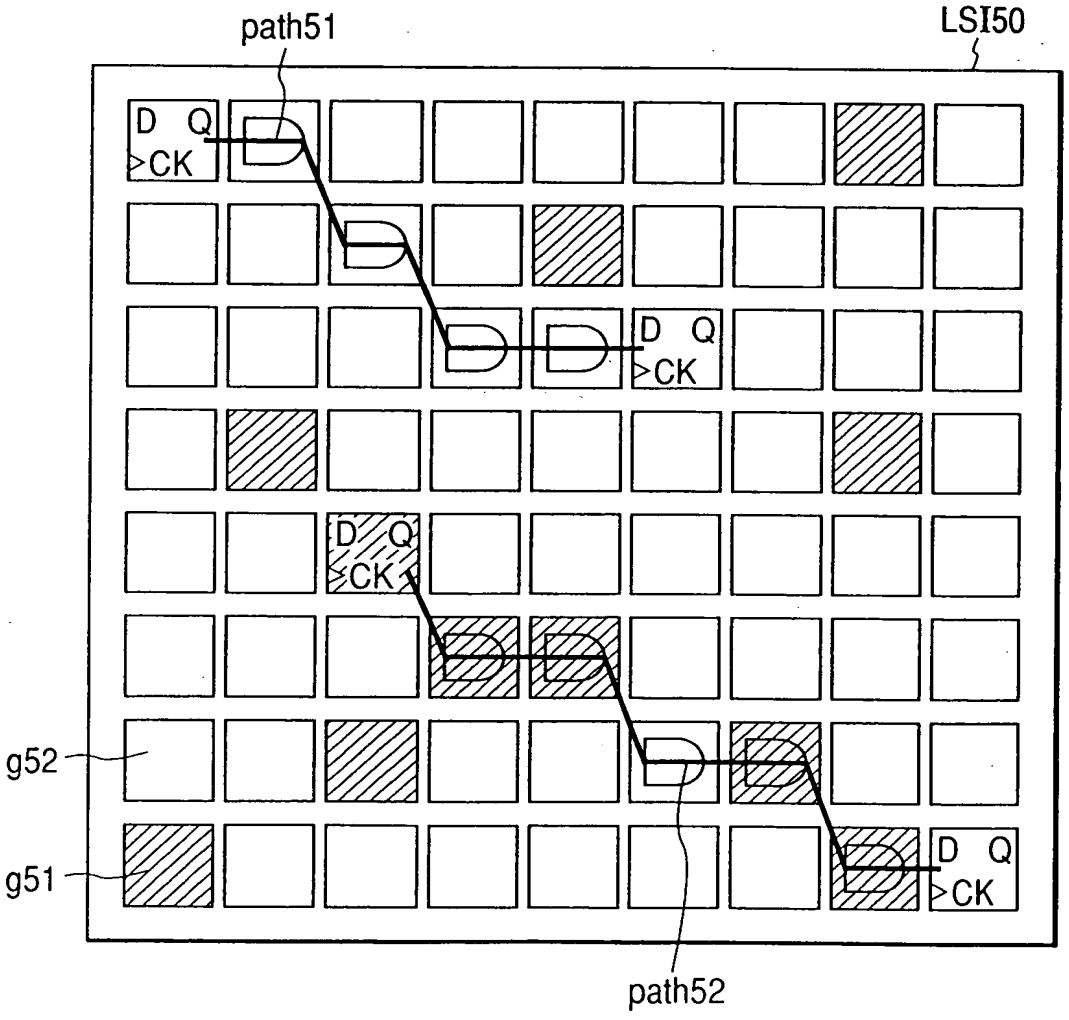

FIG. 6

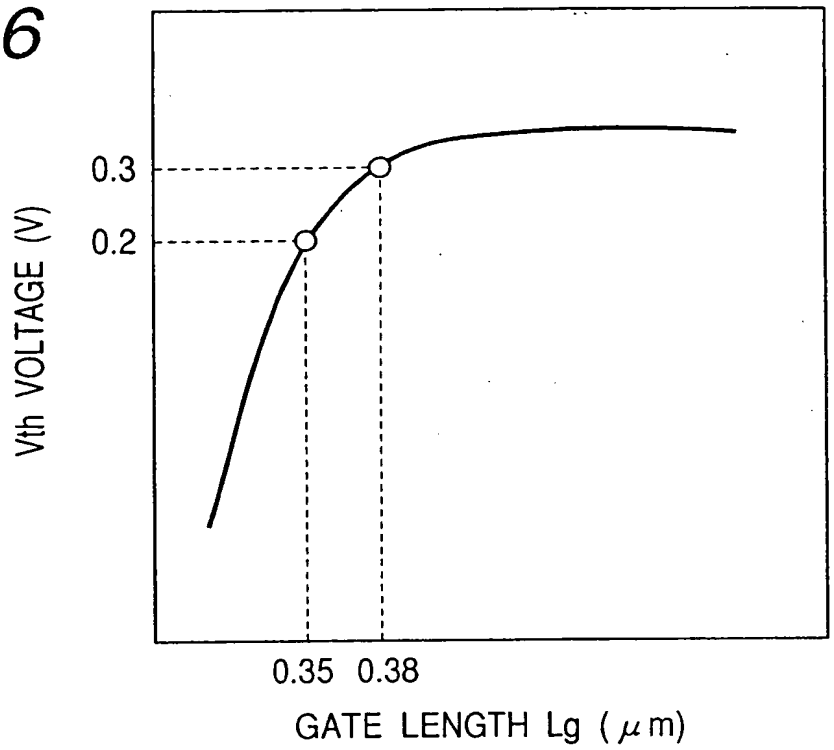
0.3
0.2
Vth VOLTAGE (V)
0.35
0.38
GATE LENGTH Lg (μm)

FIG. 7

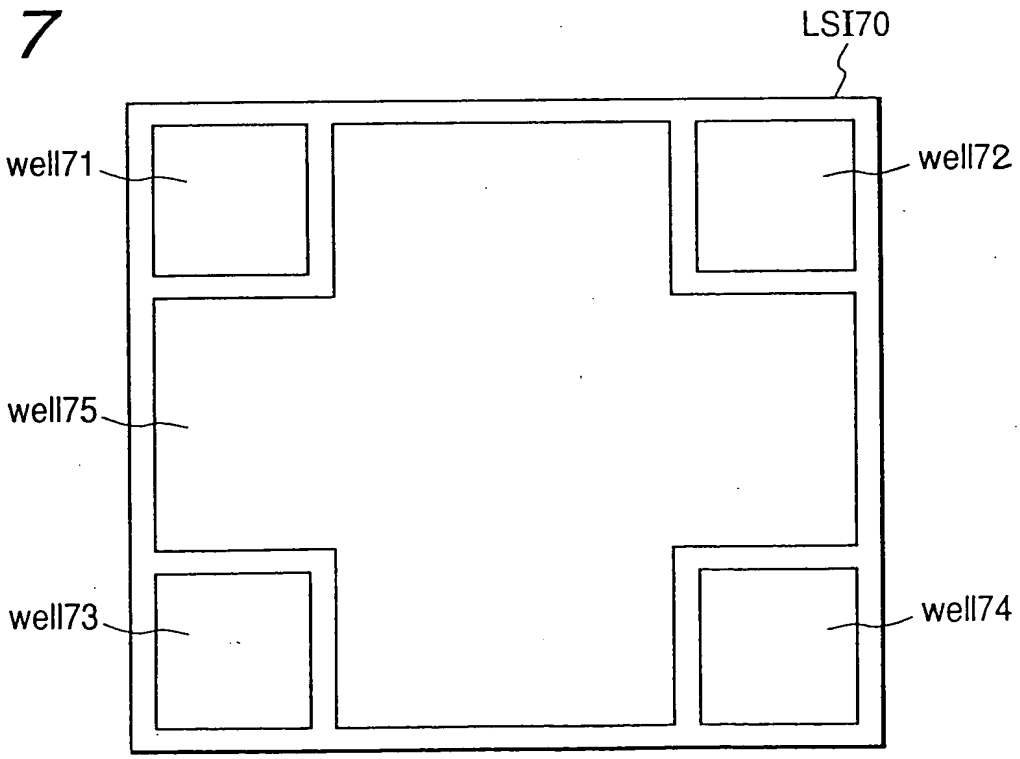
LSI70
well71
well72
well75
well73
well74

FIG. 8

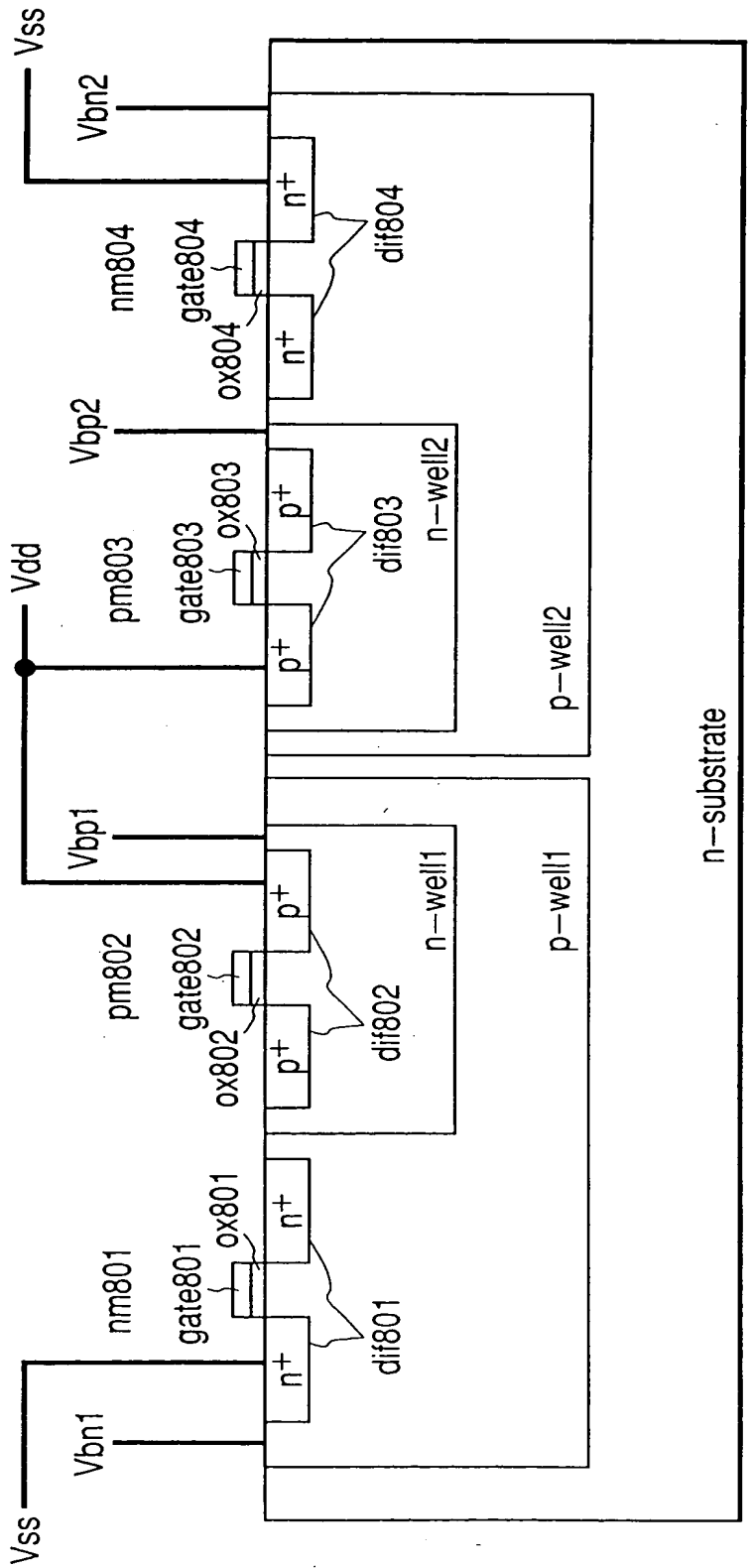
Vss
Vbn2
nm804
gate804
ox804
dif804
n+
Vbp2
Vdd
pm803
gate803
ox803
dif803
p+
n−well2
p−well2
Vbp1
pm802
gate802
ox802
dif802
n−well1
p−well1
n−substrate
nm801
gate801
ox801
dif801
Vbn1
Vss

FIG. 9(a)

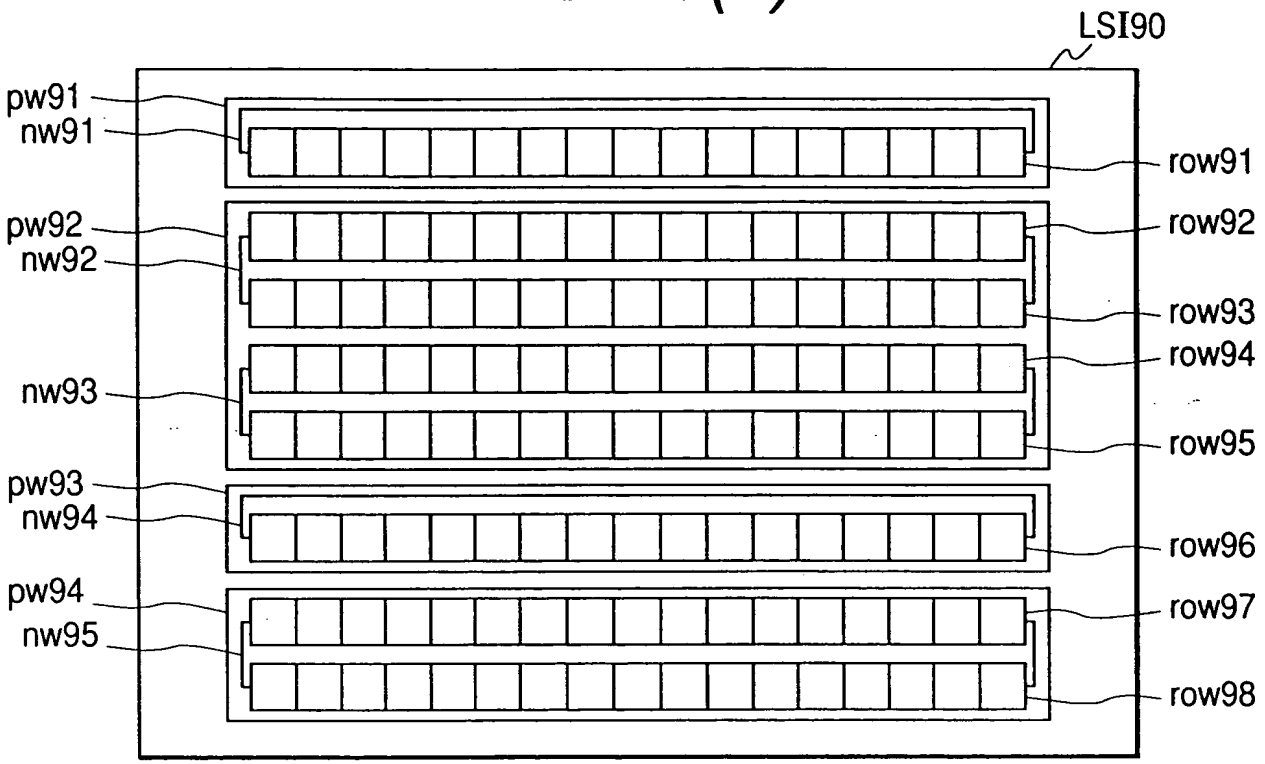
LSI90
pw91
nw91
pw92
nw92
nw93
pw93
nw94
pw94
nw95
row91
row92
row93
row94
row95
row96
row97
row98

FIG. 9(b)

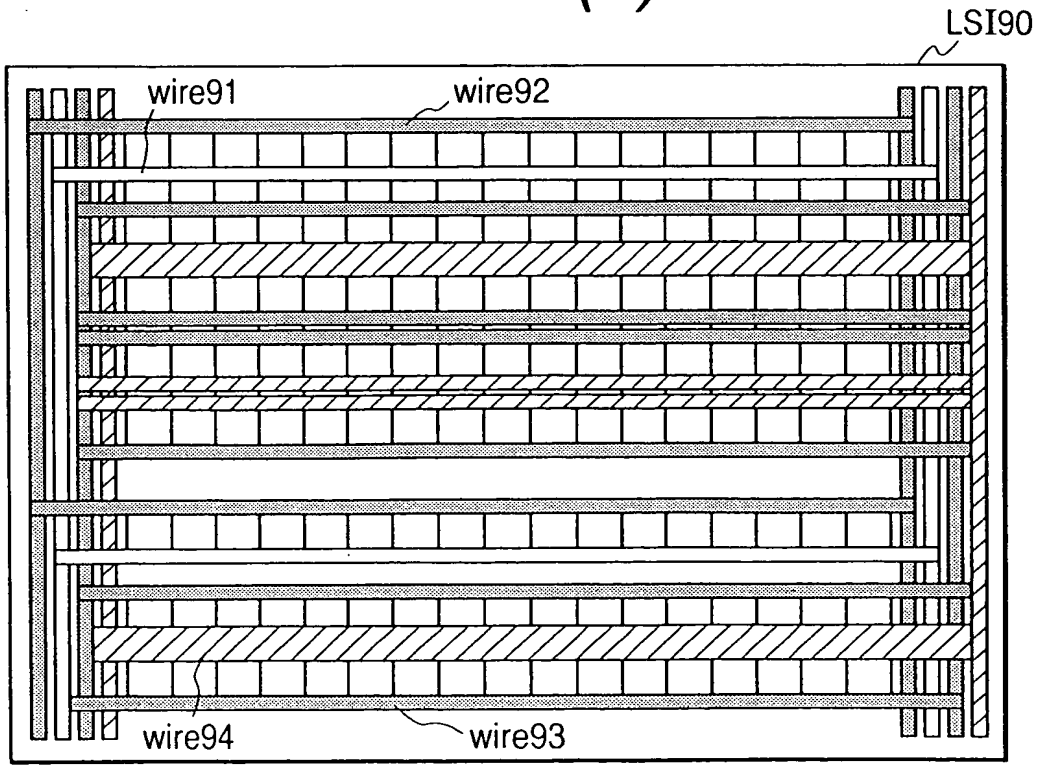
LSI90
wire91
wire92
wire94
wire93

FIG. 10

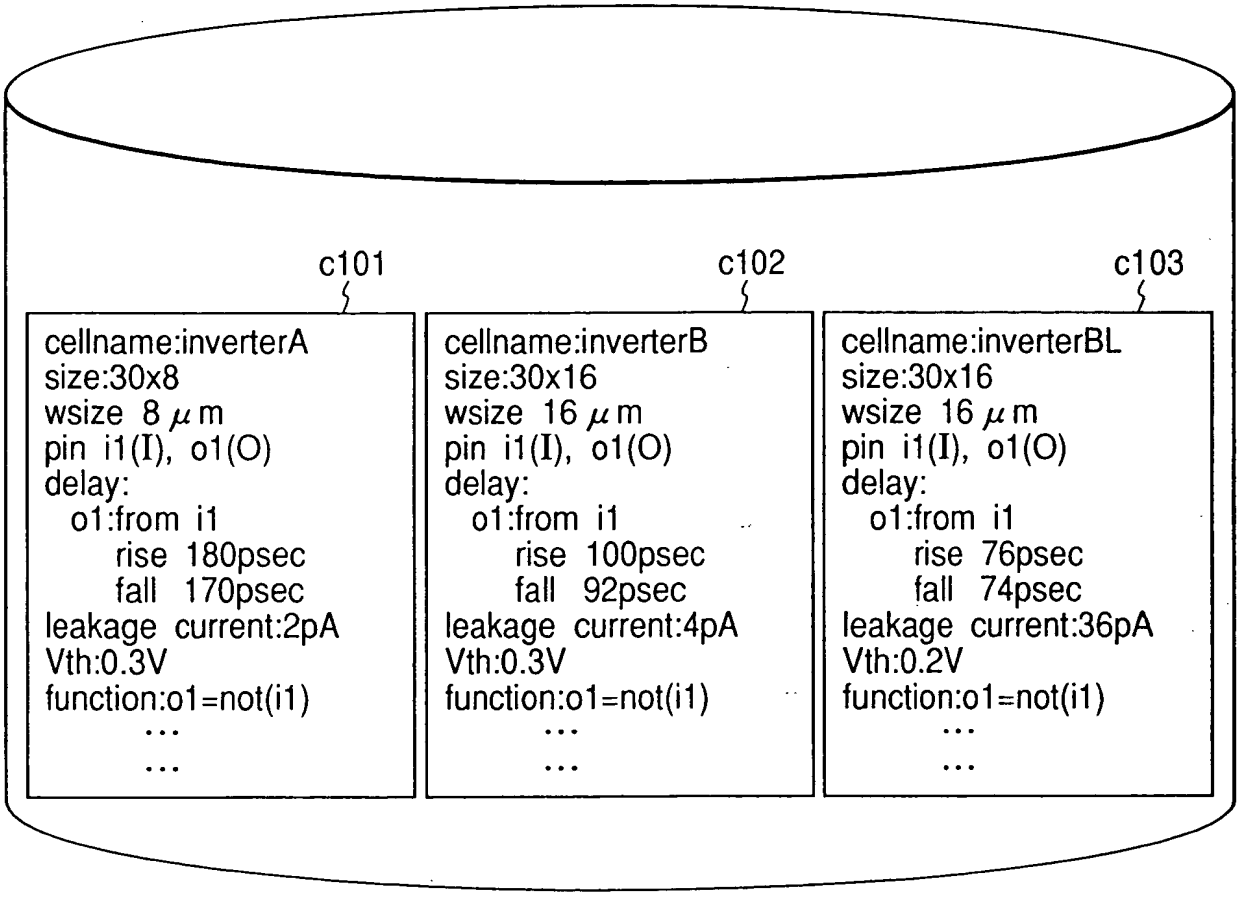
c101
cellname:inverterA
size:30x8
wsize 8 μm
pin i1(I), o1(O)
delay:
o1:from i1
rise 180psec
fall 170psec
leakage current:2pA
Vth:0.3V
function:o1=not(i1)
...
...
c102
cellname:inverterB
size:30x16
wsize 16 μm
pin i1(I), o1(O)
delay:
o1:from i1
rise 100psec
fall 92psec
leakage current:4pA
Vth:0.3V
function:o1=not(i1)
...
...
c103
cellname:inverterBL
size:30x16
wsize 16 μm
pin i1(I), o1(O)
delay:
o1:from i1
rise 76psec
fall 74psec
leakage current:36pA
Vth:0.2V
function:o1=not(i1)
...
...

FIG. 11

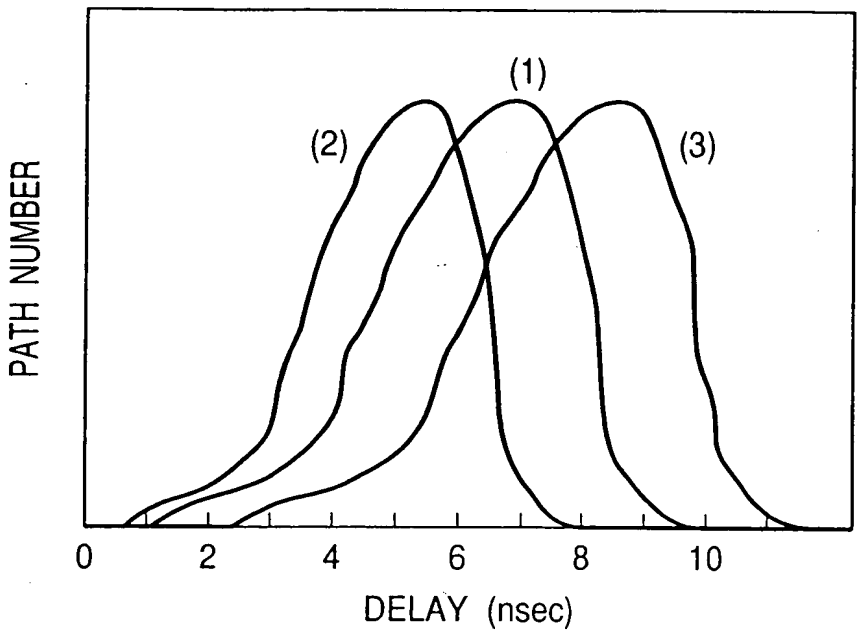
(1)
(2)
(3)
PATH NUMBER
0
2
4
6
8
10
DELAY (nsec)

FIG. 12

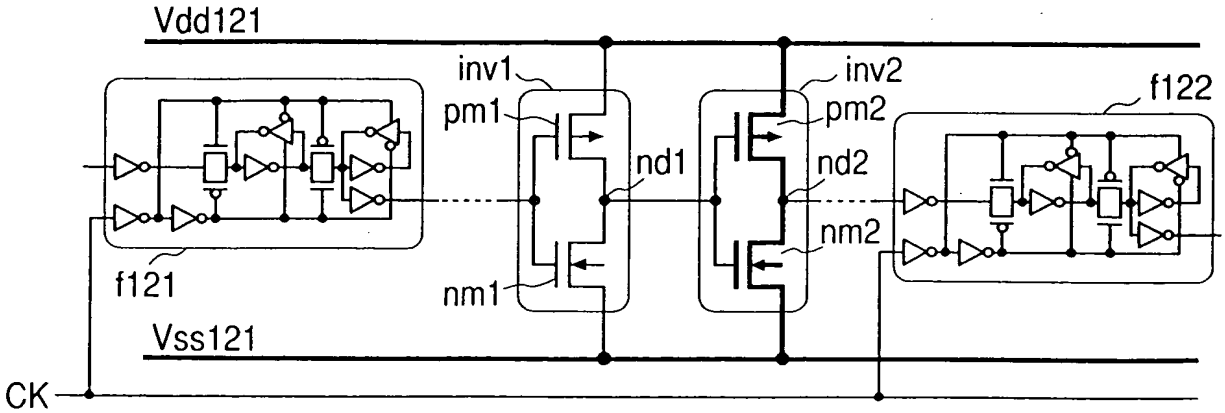
Vdd121
inv1
pm1
nd1
nm1
inv2
pm2
nd2
nm2
f121
f122
Vss121
CK

FIG. 13

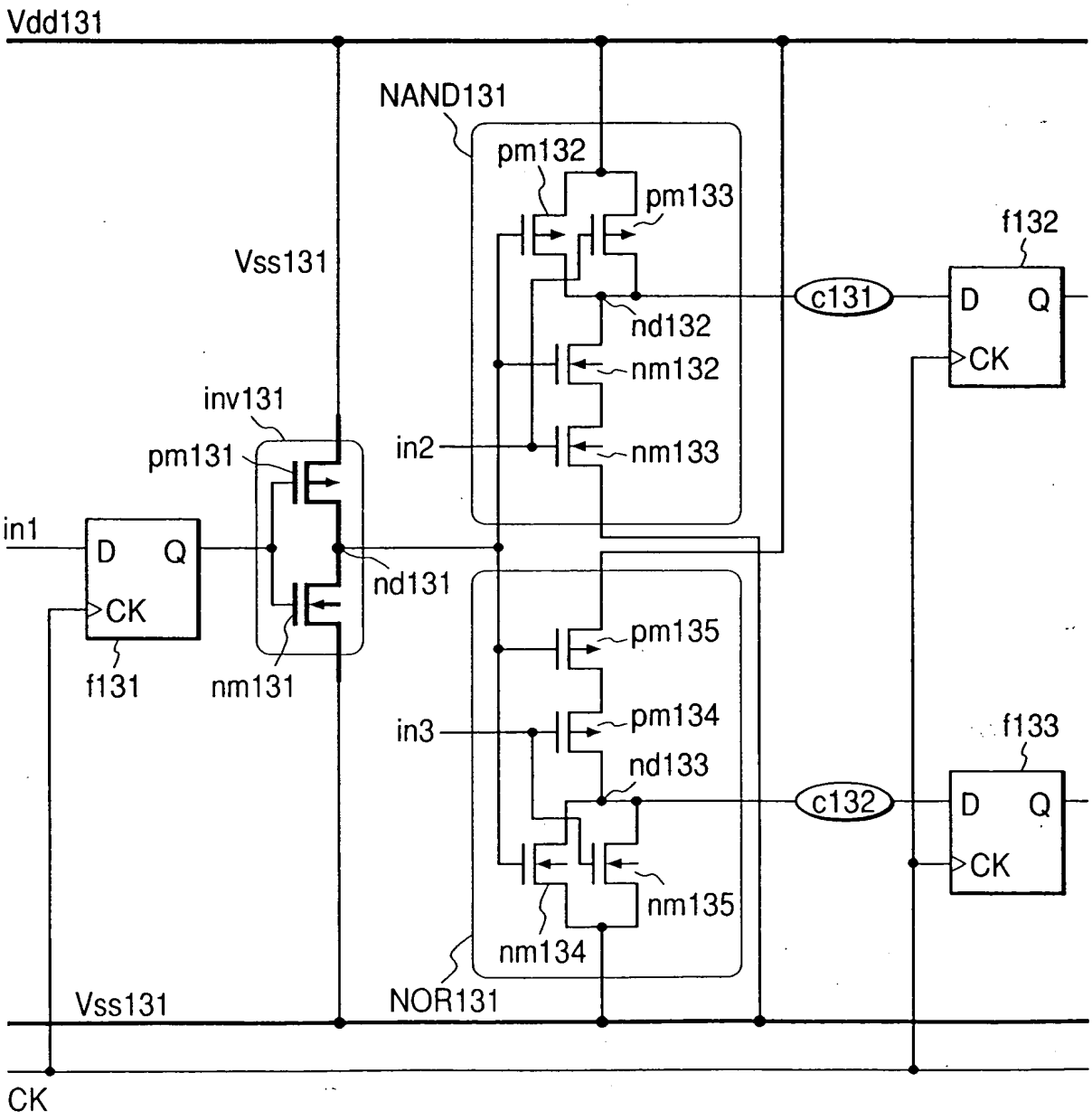
Vdd131
NAND131
pm132
pm133
f132
Vss131
c131
D
Q
nd132
CK
nm132
inv131
pm131
in2
nm133
in1
D
Q
nd131
CK
pm135
f131
nm131
in3
pm134
f133
nd133
c132
D
Q
CK
nm135
nm134
Vss131
NOR131
CK

FIG. 14

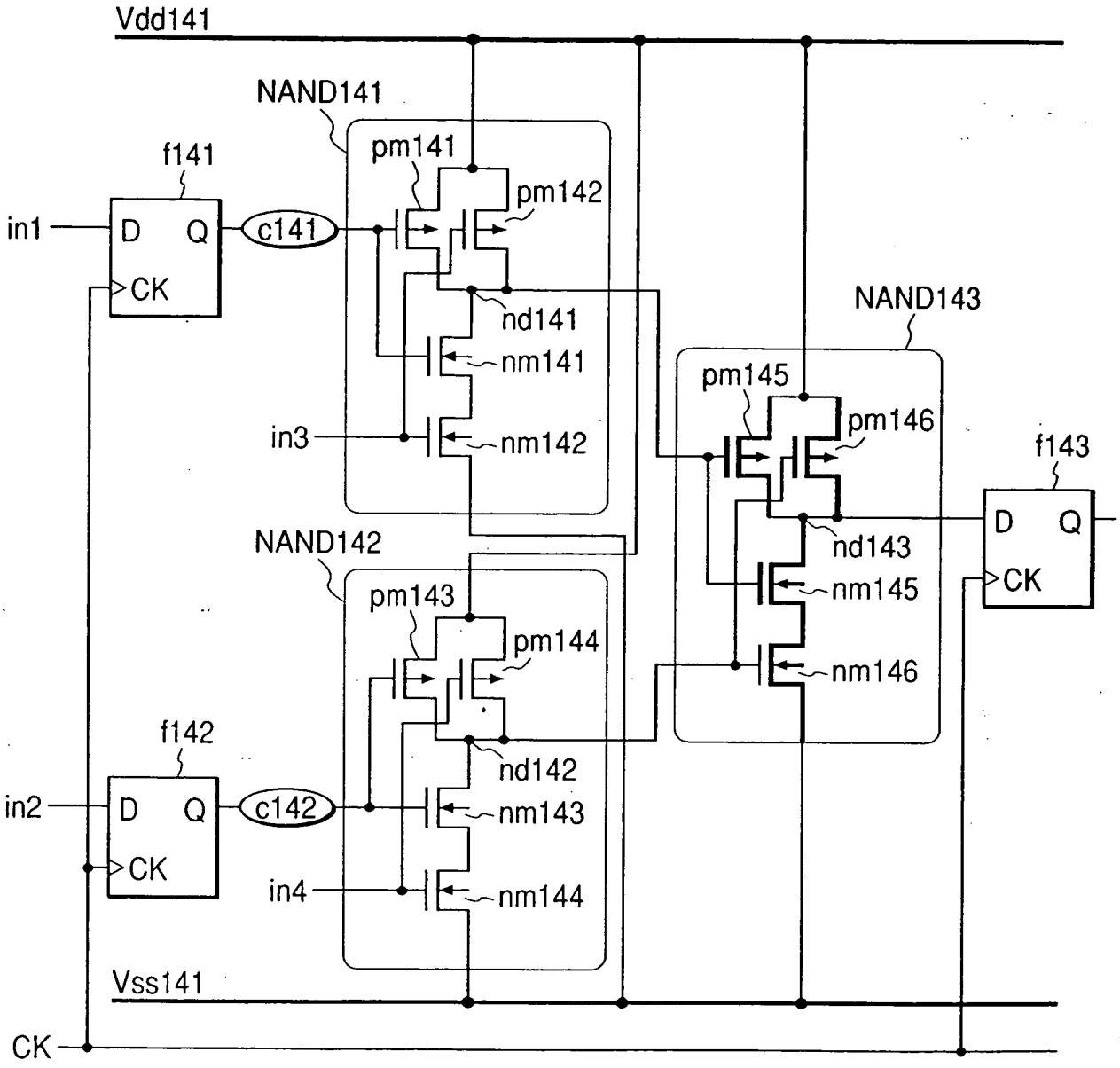
Vdd141
NAND141
pm141
pm142
f141
in1
D
Q
c141
CK
nd141
nm141
in3
nm142
NAND143
pm145
pm146
f143
D
Q
nd143
CK
nm145
NAND142
pm143
pm144
nm146
f142
nd142
in2
D
Q
c142
nm143
CK
in4
nm144
Vss141
CK

FIG. 15

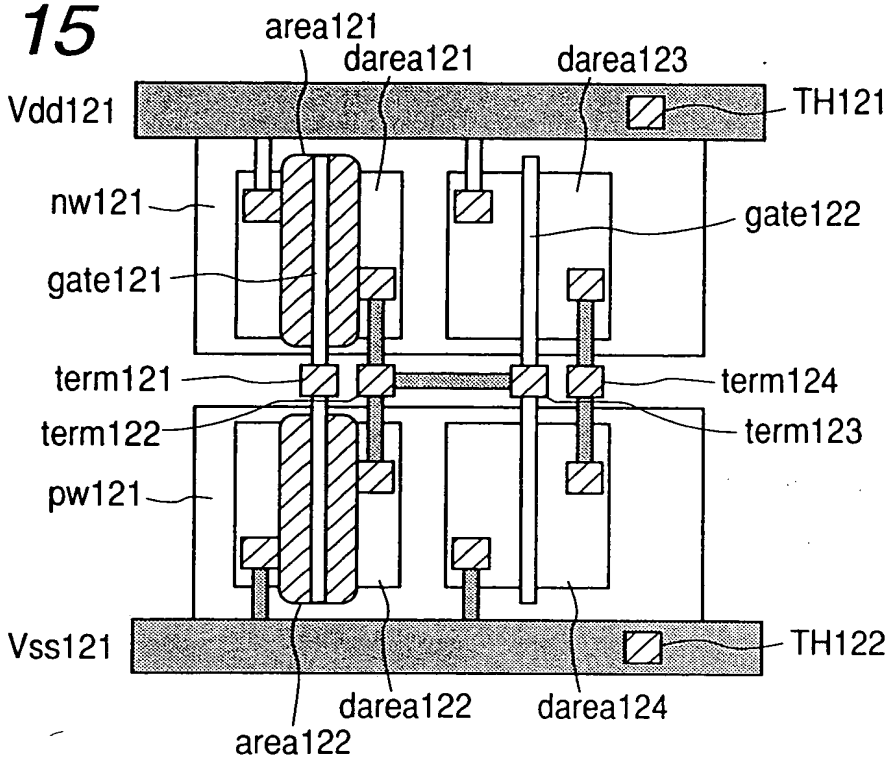
area121
darea121
darea123
Vdd121
TH121
nw121
gate122
gate121
term121
term124
term122
term123
pw121
Vss121
TH122
darea122
darea124
area122

FIG. 16

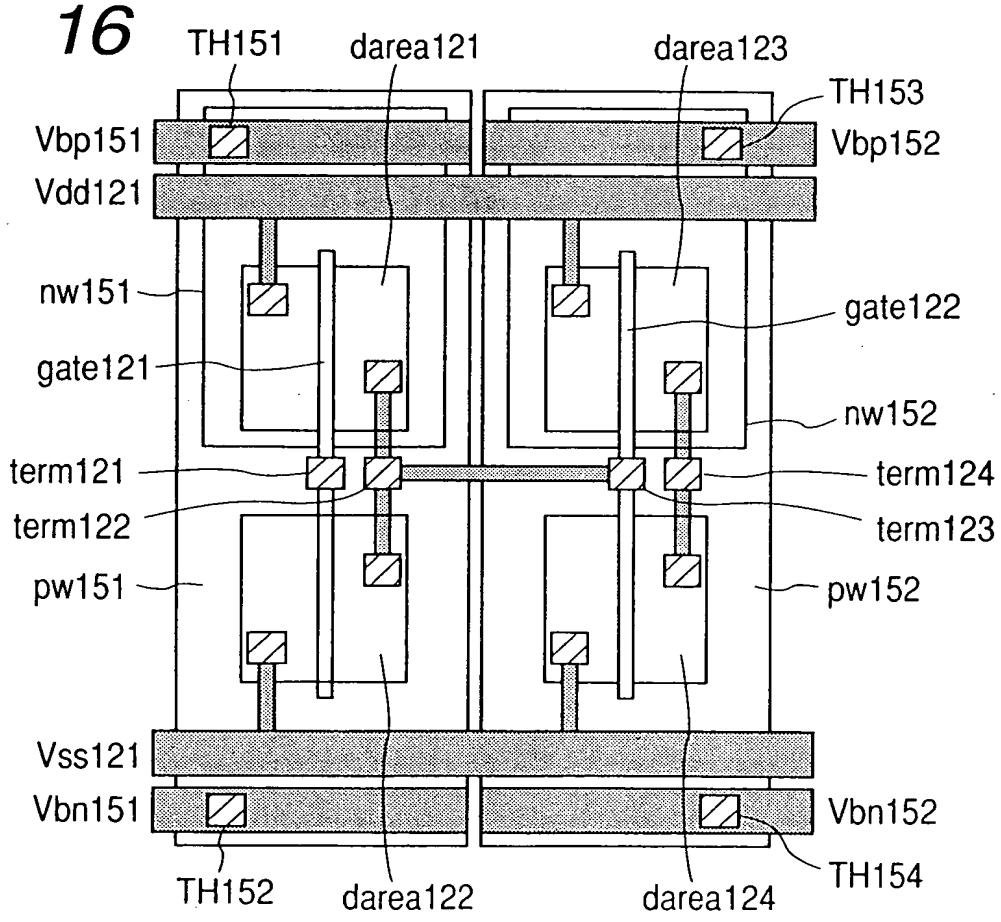
TH151
darea121
darea123
TH153
Vbp151
Vbp152
Vdd121
nw151
gate122
gate121
nw152
term121
term124
term122
term123
pw151
pw152
Vss121
Vbn151
Vbn152
TH154
TH152
darea122
darea124

FIG. 17

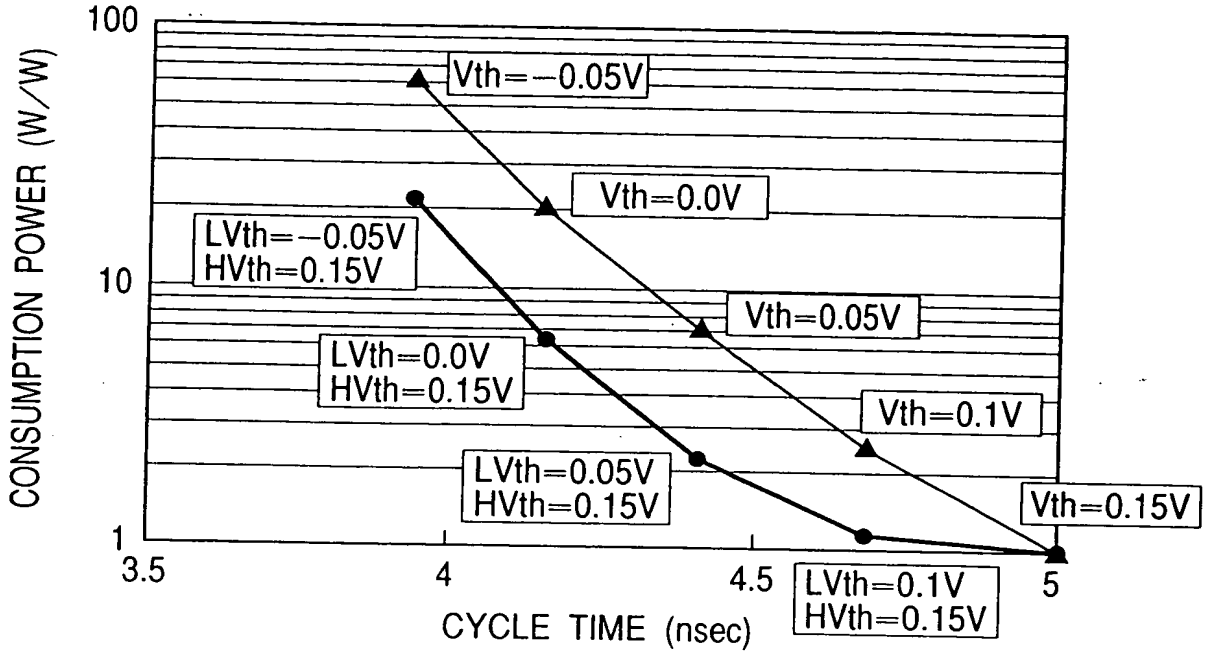
100
10
1
CONSUMPTION POWER (W/W)
Vth=−0.05V
Vth=0.0V
Vth=0.05V
Vth=0.1V
Vth=0.15V
LVth=−0.05V
HVth=0.15V
LVth=0.0V
HVth=0.15V
LVth=0.05V
HVth=0.15V
LVth=0.1V
HVth=0.15V
3.5
4
4.5
5
CYCLE TIME (nsec)

FIG. 18

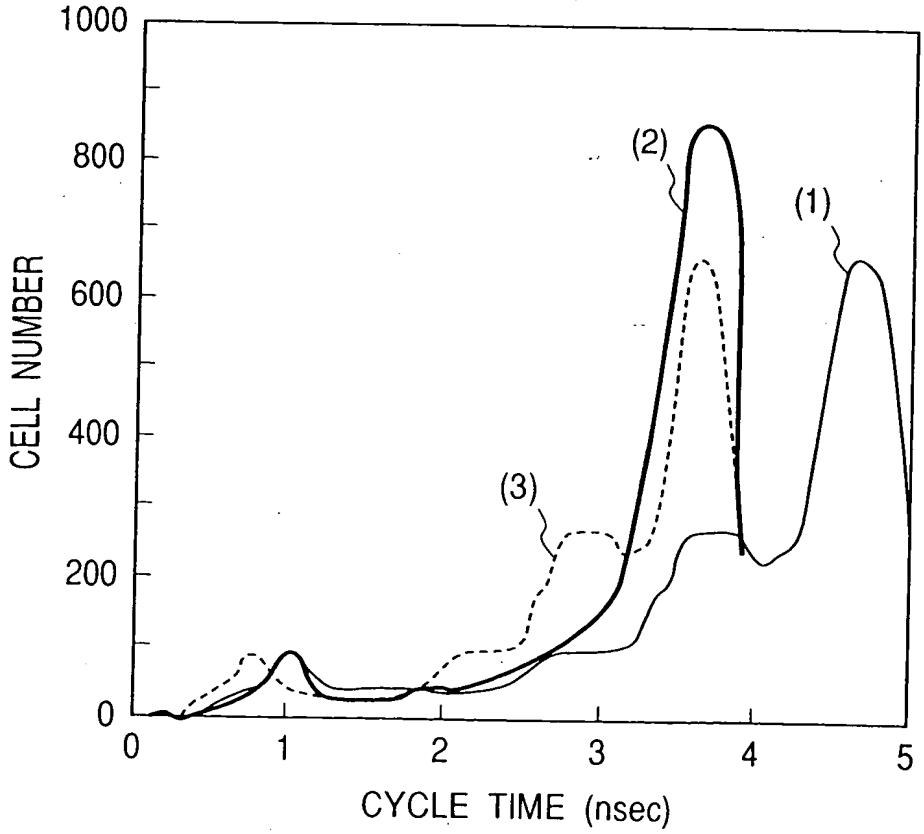
1000
800
600
400
200
0
CELL NUMBER
(1)
(2)
(3)
0
1
2
3
4
5
CYCLE TIME (nsec)

FIG. 19

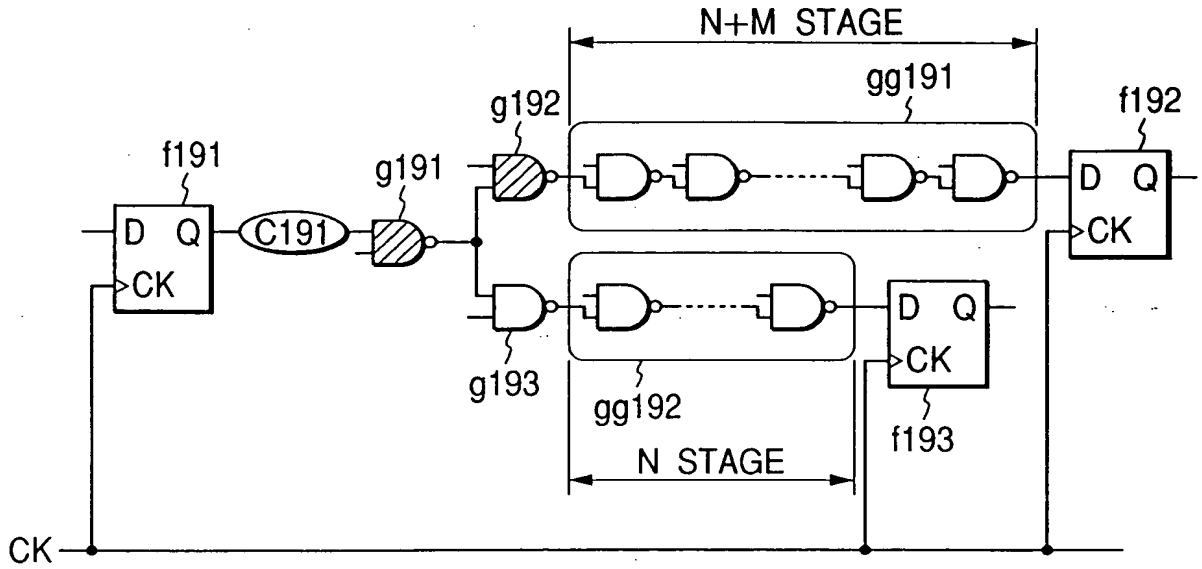
N+M STAGE
gg191
g192
f192
f191
g191
D Q
C191
CK
g193
gg192
N STAGE
f193
CK

FIG. 20

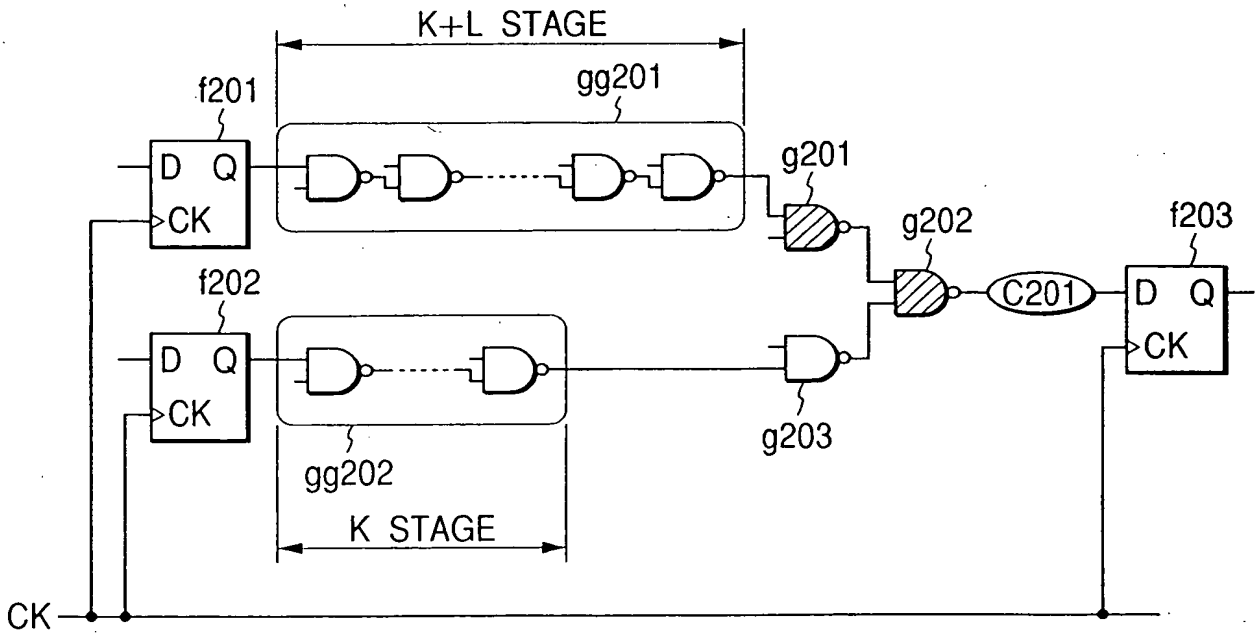
K+L STAGE
gg201
f201
g201
g202
f203
f202
D Q
C201
CK
g203
gg202
K STAGE
CK

FIG. 21

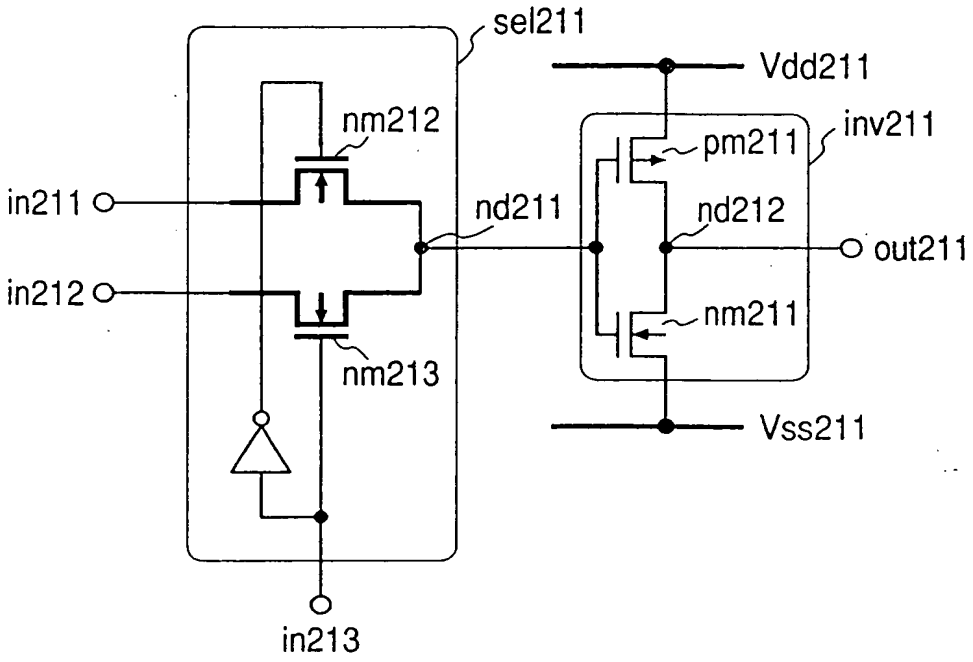
sel211
Vdd211
nm212
inv211
pm211
in211
nd211
nd212
out211
in212
nm211
nm213
Vss211
in213

FIG. 22

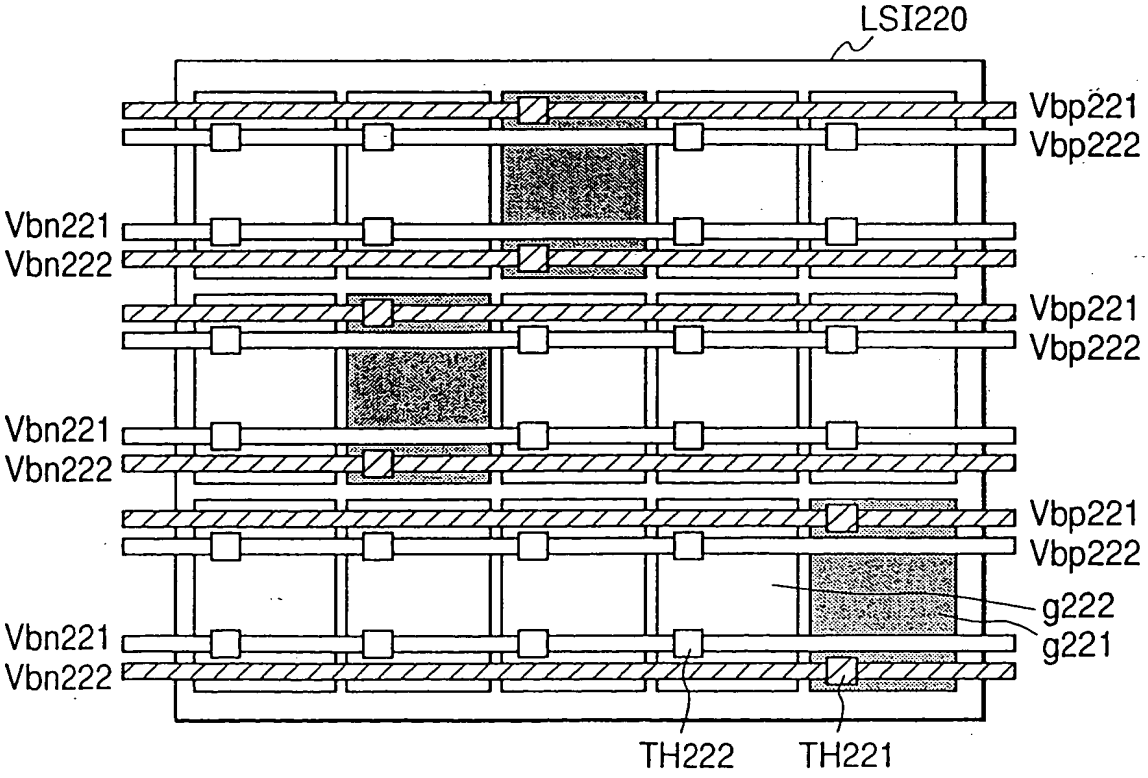
LSI220
Vbp221
Vbp222
Vbn221
Vbn222
Vbp221
Vbp222
Vbn221
Vbn222
Vbp221
Vbp222
g222
g221
Vbn221
Vbn222
TH222
TH221

FIG. 23

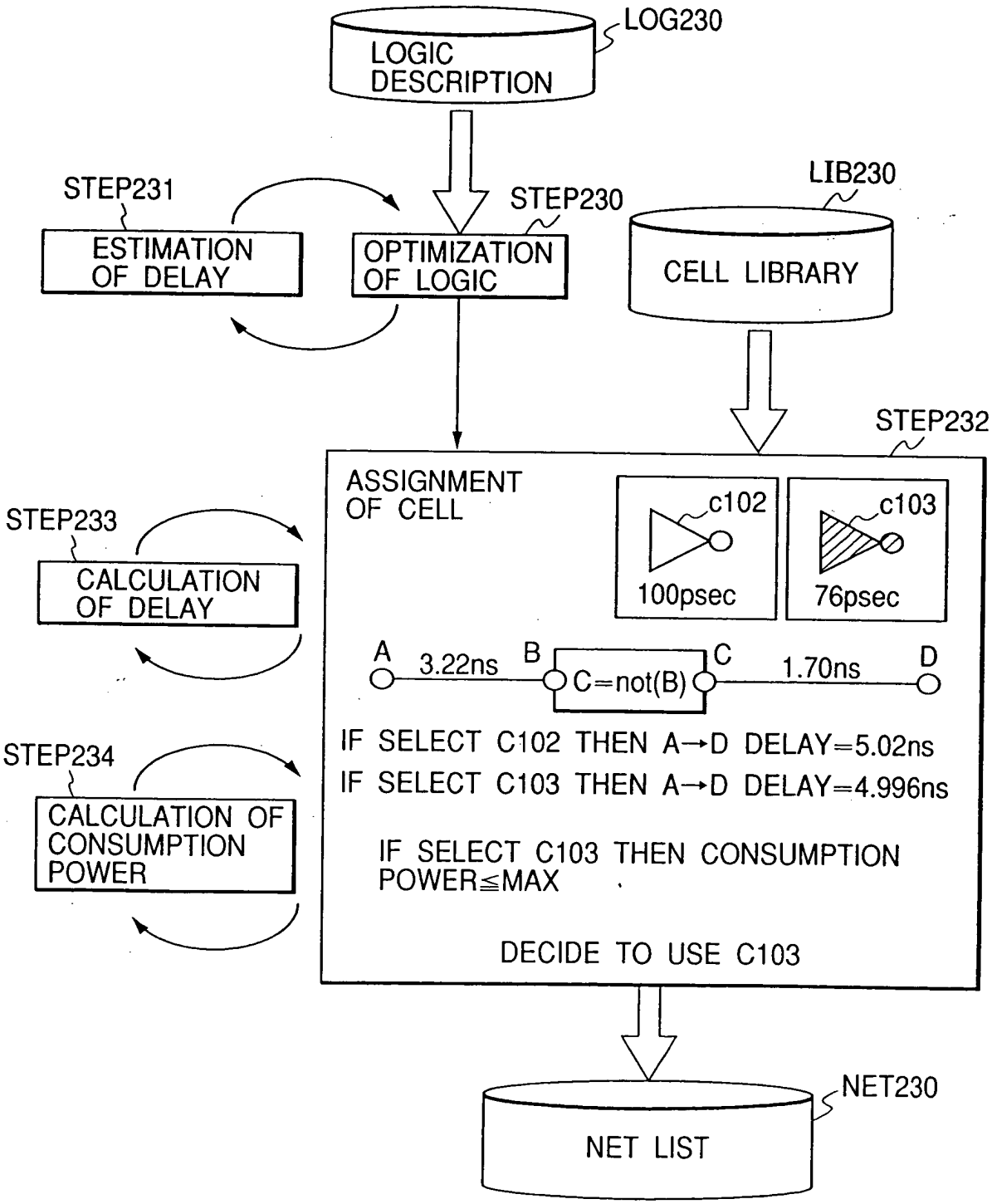
LOGIC DESCRIPTION
LOG230
STEP231
ESTIMATION OF DELAY
STEP230
OPTIMIZATION OF LOGIC
LIB230
CELL LIBRARY
STEP232
ASSIGNMENT OF CELL
c102
100psec
c103
76psec
STEP233
CALCULATION OF DELAY
A
3.22ns
B
C=not(B)
C
1.70ns
D
STEP234
CALCULATION OF CONSUMPTION POWER
IF SELECT C102 THEN A→D DELAY=5.02ns
IF SELECT C103 THEN A→D DELAY=4.996ns
IF SELECT C103 THEN CONSUMPTION POWER≦MAX
DECIDE TO USE C103
NET230
NET LIST

FIG. 24

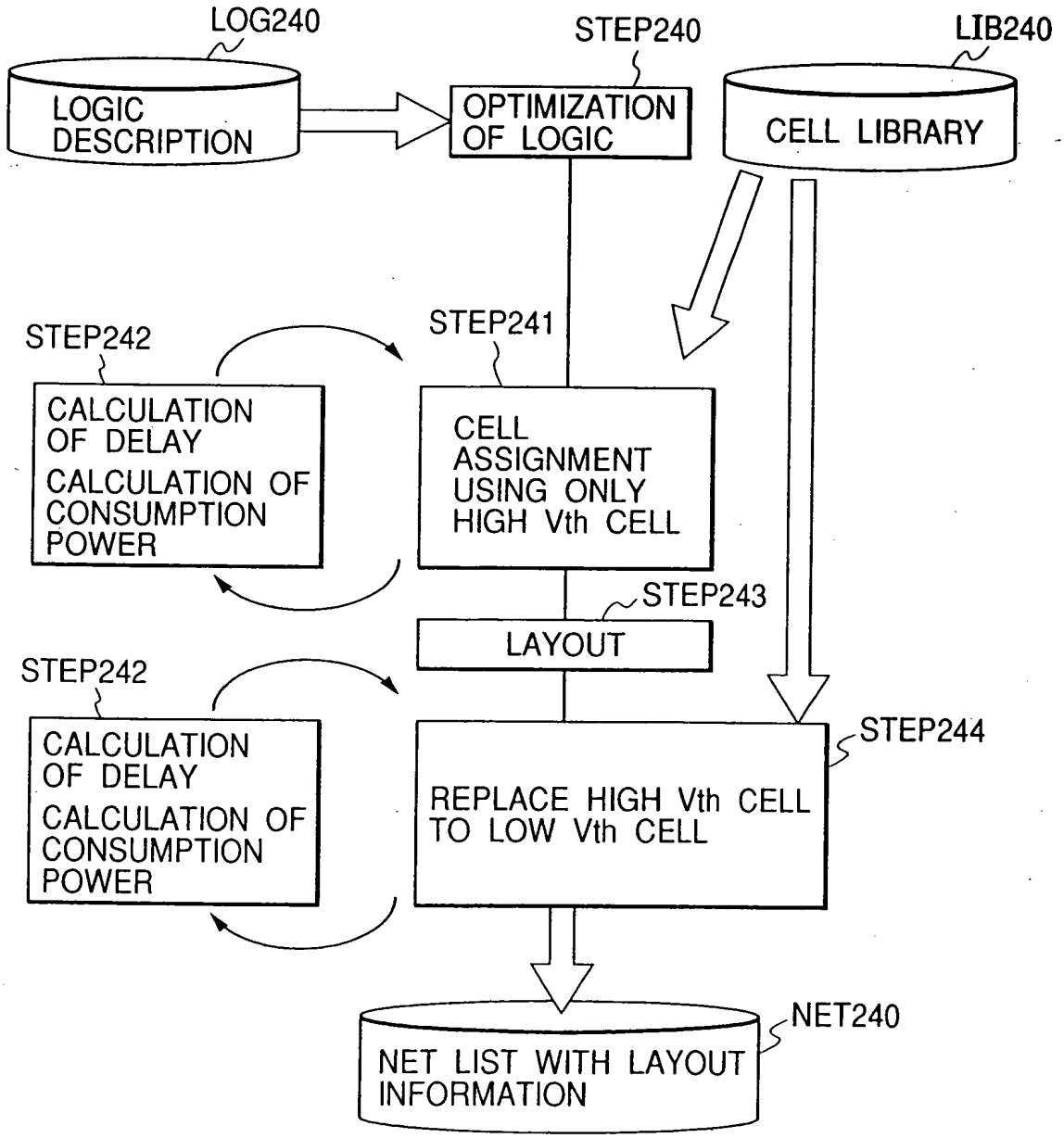
LOG240
LOGIC DESCRIPTION
STEP240
OPTIMIZATION OF LOGIC
LIB240
CELL LIBRARY
STEP242
CALCULATION OF DELAY
CALCULATION OF CONSUMPTION POWER
STEP241
CELL ASSIGNMENT USING ONLY HIGH Vth CELL
STEP243
LAYOUT
STEP242
CALCULATION OF DELAY
CALCULATION OF CONSUMPTION POWER
STEP244
REPLACE HIGH Vth CELL TO LOW Vth CELL
NET240
NET LIST WITH LAYOUT INFORMATION

FIG. 25

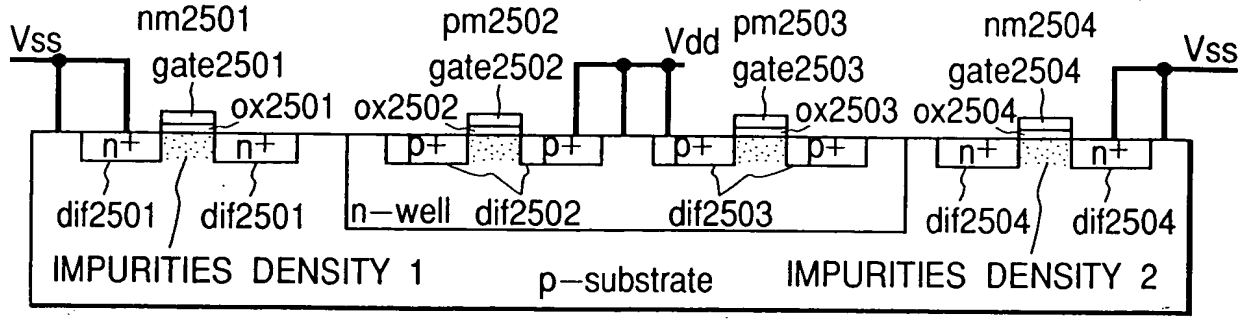

FIG. 26

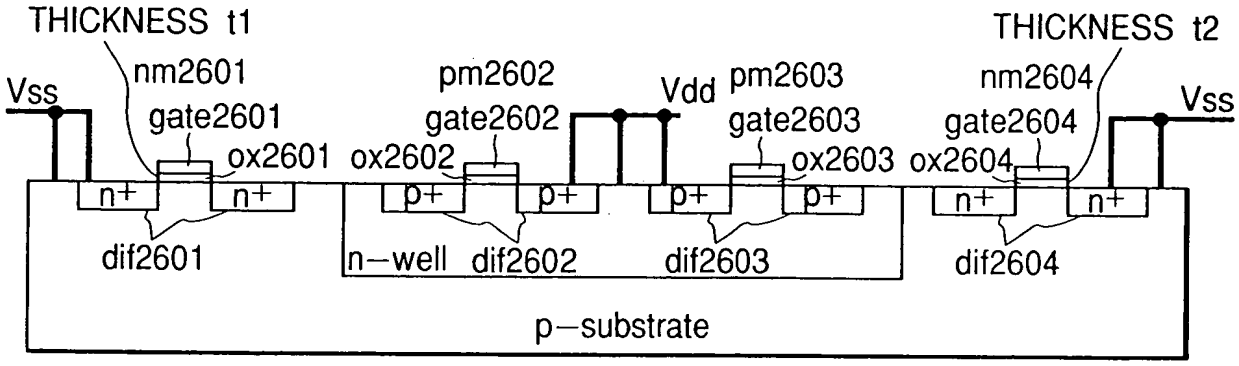

FIG. 27

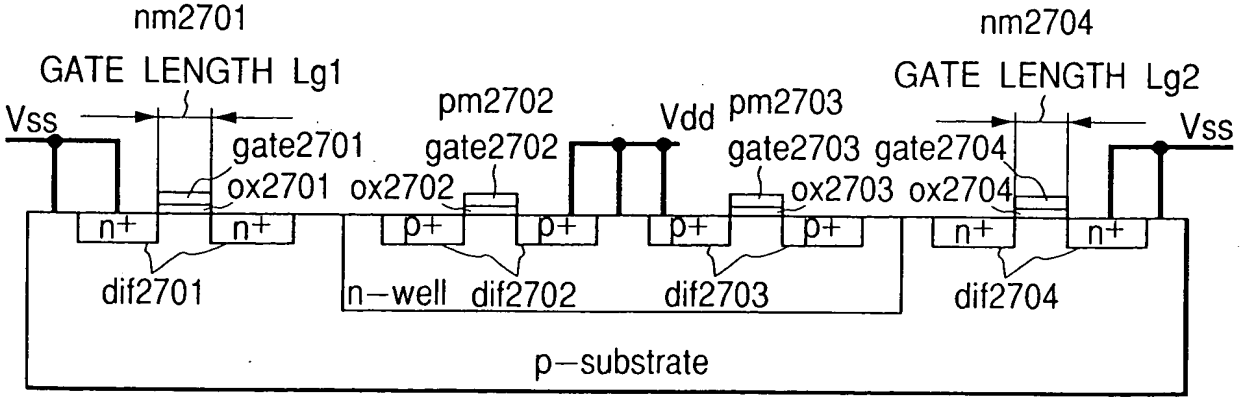
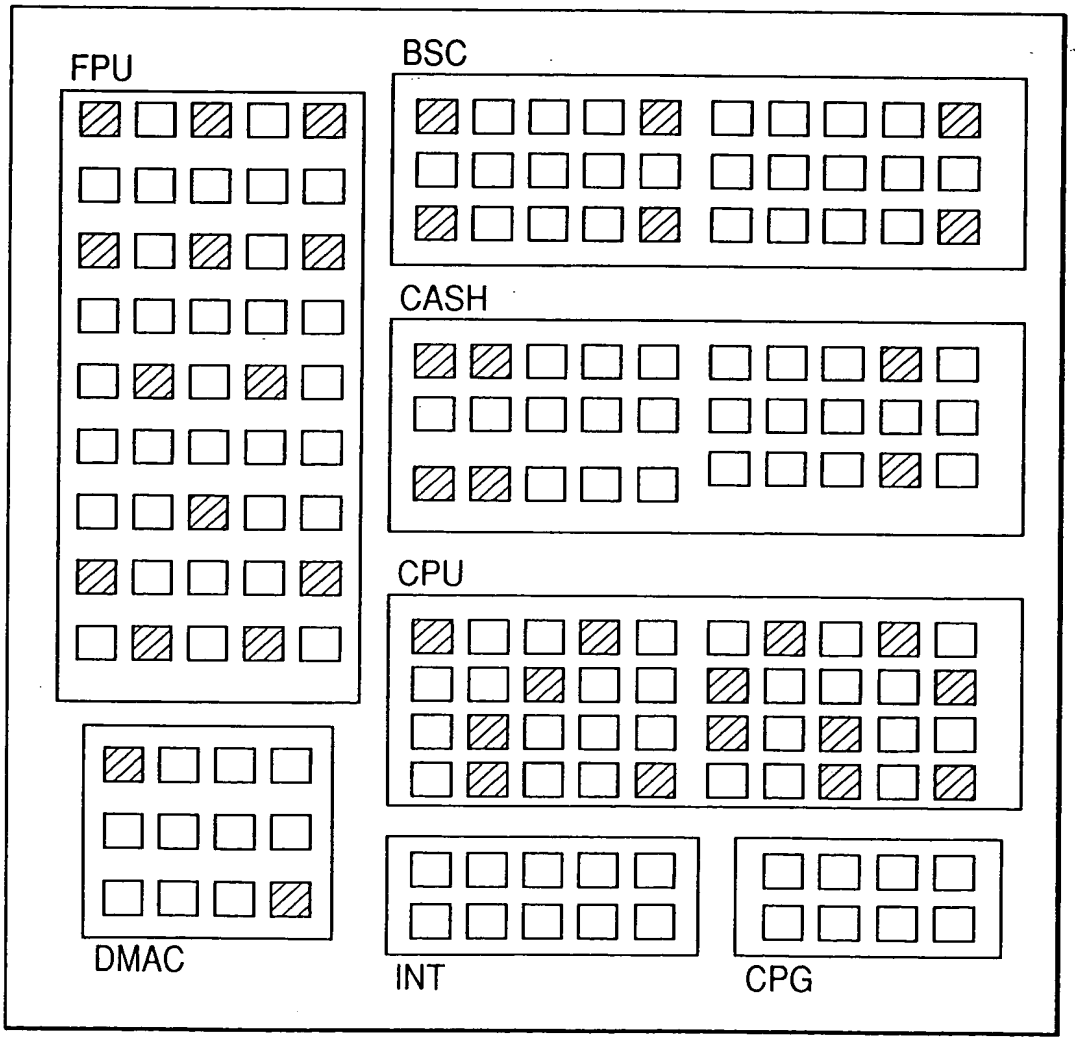
FIG. 28